Design Procedures For Millimetre Wave MMIC Voltage Controlled Oscillators

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ABSTRACT

A design procedure for millimetre wave MMIC VCOs is presented. The design uses a hierarchical breakdown of the sections of the oscillator and highlights components that should remain fixed and components which can be used to vary the oscillator performance. The method also demonstrates the use of contours of the simulated small signal conductance which are shown to be an excellent starting point for the design.

INTRODUCTION

From the circuit designers point of view, consider designing an oscillator based upon a new device for the first time. It is not immediately obvious what type or magnitude of feedback will be required to realize a one port admittance capable of generating and sustaining steady-state oscillations at the design frequency. An intuitive guess may reveal the type of feedback required but not the appropriate magnitude. This problem of getting started is overcome by considering where the areas of possible negative conductance lie in relation to the magnitude and polarity of the type of feedback being considered. Shown in Figure 1 are contours of the simulated small signal conductance at 38GHz of the synthesised one port device for varying source and gate feedback reactance values. The active device used in the simulation is a 0.2 micron gate length pHEMT with 4x15 micron fingers. The model for the device was supplied by PML as part of a design project. The device projects an f_T of 62GHz.

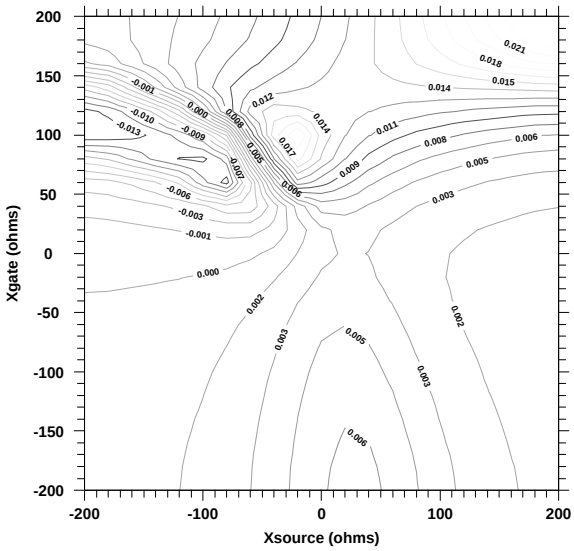

Figure 1. Contours of the simulated small signal conductance at 38GHz of the synthesised one port device for varying source and gate reactance values. Conductance is shown in Siemens.

Consideration of the area of negative conductance in the contour map indicates immediately to the designer the range of feedback available in order for oscillations to build up from noise when the device is presented with a suitable load. When via holes are to be used to short circuit the transmission lines to ground or the feedback includes lossy components such as varactor diodes, the real part

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of the feedback impedance should be included in the one port synthesis. If neither components are required then the real part may be assumed zero as the losses in the standard microstrip transmission lines will be minimal.

BIAS LINES

Bias needs to be applied to the active device and the tuning element. Poor design or positioning of bias filters can change the actual feedback from the simulated value causing the oscillator performance to depart from the predicted. The use of radial stubs as opposed to stepped impedance filters has many advantages as indicated by *Syrett*[1]. If an open circuit stub is used as a feedback element or part of the matching network, it will usually require either a dc return to ground or access to a dc supply for biasing purposes. The safest design method is to position a radial stub bias filter at the high admittance point, one quarter wavelength from the open circuit end of the stub. The bias filter should be designed to look like an RF open circuit, or very low admittance at the design centre frequency. Therefore, when the bias filter is connected in a shunt configuration to the line it will have a minimal effect on the RF performance of the section.

HIERARCHICAL DESIGN

The design procedure adopted here is to reduce the oscillator into hierarchical sections and attempt to reduce the number of variable elements required. All the transmission lines which are to carry RF signals should be fixed at a common impedance and hence transmission line width; 50Ω is popular to remove the need for discontinuities at the output. For any three terminal FET based device the one port device admittance is controlled by the feedback around the device. In this instance, source to ground feedback and gate to ground feedback are considered and illustrated as an example in Figure 2.

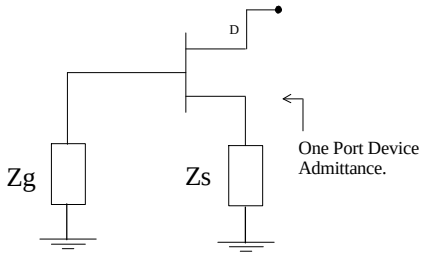

Figure 2. One port device configuration.

This type of design procedure could, however, be used for any feedback configuration. In the case of a VCO the gate feedback may be broken down into two further sections, the gate line from the device and the tuning section. The number of components in the tuning section should be minimized to include the essential elements only, as indicated in the tuning section block diagram of Figure 3.

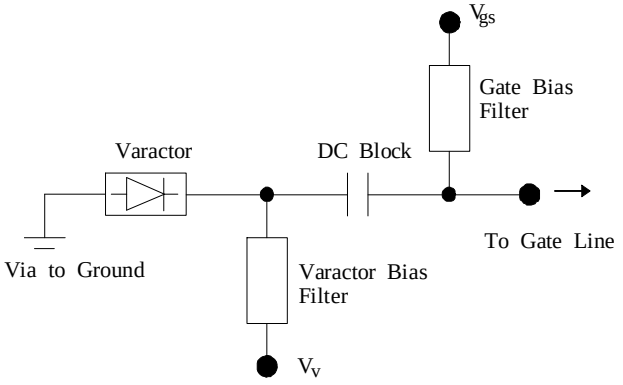

Figure 3. Block diagram of the essential elements of the tuning section.

In general these include the tuning device being grounded through a via hole, the bias filters for the varactor and the active device and a dc blocking capacitor to separate the two bias supplies. The components will undoubtedly be of varying sizes and shapes. To remove any abrupt discontinuities from the circuit, which could cause the generation of unwanted modes in the microstrip, short tapered lines should be used to

interconnect the components. It must be remembered that all foundries will employ a set of layout design rules determined by the various processes involved in the fabrication procedure. These should be kept in mind when designing each section of the oscillator. Once designed, the tuning section should be used as a *design cell* and not be physically altered. The length of the gate line however, can be varied to change the impedance seen looking into the gate feedback and so be selected to suit the design requirements. The combination of both sections would produce the *gate feedback cell*. In a similar manner the overall impedance of the source feedback can be controlled through lengths of short circuited transmission lines on the source terminals of the active device to produce the *source feedback cell*. If open circuit stubs are to be used then the procedure highlighted in the bias lines section should be employed to allow the source to be dc grounded while still retaining the required RF open circuit performance. Short circuit stubs however, are desirable for MMIC work since they take up much less space than that required for the radial stub filter section. The combination of both feedback cells and the active device forms the *one port device cell.* A single stub matching network is recommended to match to the output load to enable stable oscillations to occur. This is due to its ease of design and the fact that it enables the designer to introduce the drain dc supply without affecting the RF performance, by the use of a radial stub filter appropriately positioned on the open circuit stub.

A small signal approach for maximum power transfer is the first step to designing the matching network. As in the case of the *gate feedback cell* the *matching network cell* may be split into two cells, consisting of the *drain line cell* and the *stub cell*. The *stub cell* can be expanded further as a radial stub bias filter and a quarter wavelength open circuit stub, connected as explained in the Bias Lines section and the stub line. This hierarchical cell structure is shown in Figure 4. The bias filter section and quarter wavelength open circuit line should remain unchanged throughout the design of this cell. Only the drain line length and the stub line length should need to be altered to achieve the desired RF performance.

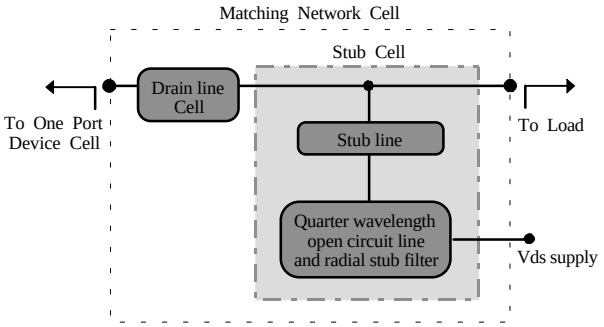

Figure 4. Breakdown of the *matching network cell* into a hierarchical cell structure.

The next step is to ensure that the oscillator will be self starting when the *one port device cell* is connected to the *matching network cell.* The output of which should be terminated in an appropriate load. A 50Ω load is common for measurement purposes, although ultimately this choice will depend upon the final system application intended for the oscillator. The simulation packages, HP EE-sof and MDS both support tools to simulate the closed loop gain around the resonator circuit, enabling the designer to check if the oscillator simulation predicts oscillations at the same frequency as the small signal design. This greatly reduces the time taken to fine tune the design compared to running a harmonic balance simulation for each alteration to the four previously mentioned transmission line sections. Once the oscillation frequency has been established the harmonic balance simulation should be employed to determine the predicted output power and harmonic content of the oscillator and the tuning range of the oscillator when the varactor voltage is varied.

CONCLUSIONS

It has been shown how the design of VCOs can be broken down into sections incorporating an excellent initial estimate of the type, magnitude and polarity of feedback required about the active device to generate areas of negative conductance. It has also been shown that the individual sections which are at times constructed of several components need only one parameter to be altered in order to change the performance of the oscillator.

It is clear from the above that for a given three terminal based active device and by using the contour mapping method to provide an initial estimate for the feedback requirements, the hierarchical cell description is an effective design strategy for high frequency oscillators.

REFERENCES

[1] Syrett, B. A. "A Novel Broad - Band Element for Device Bias and Microwave Tuning." *IEEE Trans. Microwave Theory and Techniques, vol. 28, No. 8, August 1990.* pp. 925 - 926.